REMARKS

The Examiner recommended that a flow chart of the method in Claim 1 be added to the specification. Applicant respectfully declines this suggestion. The proposed figure provided by the Examiner merely repeats the steps of Claim 1 in a block diagram, and hence, does not provide any clarification of the claimed subject matter. Applicant is not aware of any requirement that an application having a method claim directed to a method for operating a computer must include a flow chart.

The Examiner rejected Claim 1 under 35 U.S.C. 102(b) as being anticipated by US Patent 6,311,270 to Challener, *et al* (hereafter "Challener"). Applicant traverses this rejection. The Examiner has the burden of showing by reference to the cited art each claim limitation in the reference. Anticipation under 35 U.S.C. 102 requires that each element of the claim in issue be found either expressly or inherently in a single prior art reference. In re King, 231 USPQ 136, 138 (Fed. Cir. 1986); Kalman v. Kimberly-Clark Corp., 218 USPQ 781, 789 (Fed. Cir. 1983). The mere fact that a certain thing may result from a given set of circumstances is not sufficient to sustain a rejection for anticipation. *Ex parte Skinner*, 2 USPQ2d 1788, 1789 (BdPatApp&Int 1986). "When the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference" (*In re* Rijckaert, 28 USPQ2d, 1955, 1957).

With respect to Claim 1, the Examiner identifies the first processor as the content consumer, i.e., the multimedia data processing system 31. The Examiner identifies the second processor as the security program. Presumably, the Examiner is referring to the security processor 25 that is running this program, since a program is not a data processor. This leaves the service provider 11 as the third processor.

First, Challener teaches that the security processor is part of the multimedia data processing system. Hence, these are not separate processors.

Second, it should be noted that Claim 1 requires that the first and second data processors be connected by an insecure network segment. However, in the Challener system, the service provider and the security processors are the processors that are connected by the insecure network. In fact, the security processor 25 and the multimedia processor 31 do not send encrypted messages back and forth in the Challener system. Since the security processor is part of the multimedia processor, the connection between is inherently secure, since it is a communication link that is not exposed to the outside world.

Third, Applicant must disagree with the Examiner's reading of Challener. For example, the passage at col. 5, lines 20-47 does not refer to the multimedia processor 31 sending an encrypted message to security processor 25. All secure communications take place between the security processor 25 and the service provider 11, i.e., the third processor by the Examiner's assignment. Hence, Challener does not teach that the third processor forwards an encryption key to the first processor, since the first processor, i.e., multimedia processor 31 does not utilize keys in the system of Challener.

Accordingly, Applicant submits that the Examiner has not made a *primia facia* case for anticipation with respect to Claim 1 or the claims dependent therefrom.

With respect to Claim 4, the Examiner has not pointed to any teaching of the first processor, i.e., the multimedia processor, sending any message to the security processor, no less one that causes the security processor to request a key from the third processor. Hence, there are additional grounds for allowing Claim 4.

With respect to Claim 6, the Examiner has not pointed to any teaching in Challener in which the first and third processors include a local area network. The passage at col. 2, lines 61-64 referenced by the Examiner certainly does not refer to a local area network. Hence, there are additional grounds for allowing Claim 6.

With respect to Claim 7, the Examiner maintains that Challener teaches that the first and third processors are connected by a network segment that has a higher level of security than the insecure network. The passage cited by the Examiner at col. 2, line 53-57 does not refer to any network segment other than the insecure segment 15. In fact, Challener only refers to one network segment. Hence, there are additional grounds for allowing Claim 7.

Regarding Claim 8, the Examiner stated that the "first encryption protocol requires less computational resources than said second encryption protocol" is met by Challener in the passage at col. 5, line 33-47. Applicant must disagree. The passage does not teach anything with respect to the computational resources needed for the particular forms of encryption protocols taught therein. Accordingly, there are additional grounds for allowing Claim 8.

I hereby certify that this paper is being sent by FAX to 571-273-8300.

Respectfully Submitted,

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